CLAIMS:

1. A post-processing method for correcting media noise errors and producing a corrected recovered data output signal, for use in a sampled data read channel of a mass data storage device that has a Viterbi detector that receives actual sampled partial response target data from a data medium of the mass data storage device, comprising:

filtering a recovered partial response target signal derived from said recovered data output signal and said sampled partial response target data to produce a filtered output signal;

providing a threshold circuit to provide a threshold against which said filtered output signal is compared;

adding a predetermined value to the filtered output signal when a predetermined error event pattern due to media noise occurs in said recovered data output signal;

and modifying the recovered data output signal when said filtered output signal exceeds the threshold of said threshold circuit.

2. The method of claim 1 wherein said Viterbi detector is an EPR4 Viterbi detector.

3. The method of claim 1 wherein said Viterbi detector is an EEPR4 Viterbi detector.

4. The method of claim 1 wherein said error event pattern is ex = ±{1}.

5. The method of claim 1 wherein said error event pattern is ex = ±{1-1}.

6. The method of claim 1 wherein said filtering is accomplished by applying said output to an FIR filter.

7. The method of claim 1 wherein said predetermined value in an EPR4 channel is -A when said predetermined error event pattern is "1X1".

8. The method of claim 1 wherein said predetermined value in an EPR4 channel is +A when said predetermined error event pattern is "0X0".

9. The method of claim 1 wherein said predetermined value in an EPR4 channel is 0 when said predetermined error event pattern is other than "1X1" or "0X0".

10. The method of claim 1 wherein said predetermined value in an EEPR4 channel is determined from the following tables:

Recovered Write Current $\hat{c}(k)$								Output
k	-3	-2	-1	0	1	2	3	
	X	0	0	X	0	0	X	Ajitter
	1	1	0	X	0	0	X	
	X	0	0	X	0	1	1	
	X	1	1	X	1	1	X	-Ajitter
	0	0	1	X	1	1	X	
	X	1	1	X	1	0	0	
Others								0

Polarity Check				Correction	
Amplitude	Polarity	$\hat{c}(0)$	$\hat{c}(1)$	$\hat{c}(0)$	$\hat{c}(1)$
$\lvert fexA(6) \rvert > VthA$	$FexA(6) > 0$	0	X	1	X
	$FexA(6) < 0$	1	X	0	X
$\lvert FexB(6) \rvert > VthA$	$FexA(6) > 0$	0	1	1	0
	$FexA(6) < 0$	1	0	0	1

wherein the polarity check correction table is logically or'd with the output of the recovered write current $\hat{c}(k)$ table to produce a correction value.

11. The method of claim 1 wherein said predetermined value in an EPR4 channel is determined from the following table:

Recovered Write Current $\hat{c}(k)$				Output
k	-1	0	1	
	0	X	0	Ajitter
	1	X	1	-Ajitter
Others				0

and the polarity is determined from the following table:

Polarity check		Correction	
Amplitude	Polarity		
$\|fexA\| > VthA$	$FexA > 0$	0	1
	$FexA < 0$	1	0

12. A sampled data detection technique for use in a mass data storage device for correcting for media noise, comprising:

detecting an actual sampled partial response target from a transducer head of said mass data storage device which has been equalized to a partial response level of at least EPR4 in a Viterbi detector having a partial response detection level of at least EPR4 to produce a recovered data output signal;

delaying said actual sampled partial response target signal for a time substantially equal to a time required by said Viterbi detector to generate said recovered data output signal from said actual sampled partial response target signal to produce a delayed actual sampled partial response target signal;

converting said recovered data output signal to a partial response level of said actual sampled data output signal to produce a converted recovered partial response target signal;

subtracting said converted recovered partial response target signal from said delayed actual sampled partial response target signal to produce an error signal;

determining the occurrence of a predetermined error event pattern in said recovered data output signal to produce a filtered output signal;

adding a predetermined value to the filtered output signal when a predetermined error event pattern due to media noise occurs in said recovered data output signal;

and modifying the recovered data output signal when said filtered output signal exceeds the threshold of said threshold circuit.

13. The method of claim 12 wherein said producing a detection signal comprises filtering said error signal with an FIR filter.

14. The method of claim 12 wherein said determining the occurrence of a predetermined error event pattern in said recovered data output signal comprises determining the occurrence of ex = ±{1} in said recovered data output signal.

15. The method of claim 12 wherein said determining the occurrence of a predetermined error event pattern in said recovered data output signal comprises determining the occurrence of ex = ±{1-1} in said recovered data output signal.

16. The method of claim 12 wherein said predetermined value in an EEPR4 channel is determined from the following tables:

Recovered Write Current $\hat{c}(k)$								Output
k	-3	-2	-1	0	1	2	3	
	X	0	0	X	0	0	X	Ajitter
	1	1	0	X	0	0	X	
	X	0	0	X	0	1	1	
	X	1	1	X	1	1	X	-Ajitter
	0	0	1	X	1	1	X	
	X	1	1	X	1	0	0	
Others								0

Polarity Check				Correction	
Amplitude	Polarity	$\hat{c}(0)$	$\hat{c}(1)$	$\hat{c}(0)$	$\hat{c}(1)$
$\|fexA(6)\| > VthA$	$FexA(6) > 0$	0	X	1	X
	$FexA(6) < 0$	1	X	0	X
$\|FexB(6)\| > VthA$	$FexA(6) > 0$	0	1	1	0
	$FexA(6) < 0$	1	0	0	1

wherein the polarity check correction table is logically or'd with the output of the recovered write current $\hat{c}(k)$ table to produce a correction value.

17. The method of claim 12 wherein said predetermined value in an EPR4 channel is determined from the following table:

Recovered Write Current $\hat{c}(k)$				Output
k	-1	0	1	
	0	X	0	Ajitter
	1	X	1	-Ajitter
Others				0

and the polarity is determined from the following table:

Polarity check		Correction	
Amplitude	Polarity		
$\|fexA\| > VthA$	$FexA > 0$	0	1
	$FexA < 0$	1	0

18. A post-processor circuit for use in a sampled data read channel of a mass data storage device of the type using a Viterbi detector that receives an actual sampled partial response target signal from a storage medium of said mass data storage device to produce a recovered data output signal, comprising:

an error pattern detector to generate an error pattern event indicating signal if a predetermined error event pattern occurs in said sampled partial response target signal;

a circuit for generating an error signal based upon a difference between said recovered data output signal and a delayed said actual sampled partial response target signal;

a circuit for adding a predetermined value to the error signal when a predetermined error event pattern due to media noise occurs in said recovered data output signal;

a threshold circuit to generate an error correction control signal if a magnitude of said error signal exceeds a predetermined threshold;

and an error correction circuit to modify the recovered data output signal when said error correction control signal and said error event pattern indicating occurrence signal are generated.

19. The circuit of claim 18 wherein said predetermined error pattern event is ex = ±{1}.

20. The circuit of claim 18 wherein said predetermined error pattern event is ex = ±{1-1}.

21. The circuit of claim 18 wherein said circuit for generating an error signal is an FIR filter

22. The circuit of claim 18 wherein said Viterbi detector has a partial response level of at least EPR4.

23. The circuit of claim 18 wherein said Viterbi detector has a partial response level of at least EEPR4.

24. The method of claim 18 wherein said predetermined value in an EEPR4 channel is determined from the following tables:

Recovered Write Current $\hat{c}(k)$								Output
k	-3	-2	-1	0	1	2	3	
	X	0	0	X	0	0	X	Ajitter
	1	1	0	X	0	0	X	
	X	0	0	X	0	1	1	
	X	1	1	X	1	1	X	-Ajitter
	0	0	1	X	1	1	X	
	X	1	1	X	1	0	0	
Others								0

Polarity Check				Correction	
Amplitude	Polarity	$\hat{c}(0)$	$\hat{c}(1)$	$\hat{c}(0)$	$\hat{c}(1)$
$\lvert fexA(6) \rvert > VthA$	$FexA(6) > 0$	0	X	1	X
	$FexA(6) < 0$	1	X	0	X
$\lvert FexB(6) \rvert > VthA$	$FexA(6) > 0$	0	1	1	0
	$FexA(6) < 0$	1	0	0	1

wherein the polarity check correction table is logically or'd with the output of the recovered write current $\hat{c}(k)$ table to produce a correction value.

25. The method of claim 18 wherein said predetermined value in an EPR4 channel is determined from the following table:

Recovered Write Current $\hat{c}(k)$				Output
k	-1	0	1	
	0	X	0	Ajitter
	1	X	1	-Ajitter

Others	0

and the polarity is determined from the following table:

Polarity check		Correction	
Amplitude	Polarity		
$\|fexA\| > VthA$	$FexA > 0$	0	1
	$FexA < 0$	1	0